AP-705

APPLICATION NOTE

Feature Set Comparison of the 80C186 Family and the Intel386™ EX Embedded Processor

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1.0 PURPOSE OF THIS APPLICATION NOTE

Today's embedded applications are moving toward higher performance, higher integration, and increased addressability. With the introduction of the Intel386™ EX embedded processor, designers have a logical and cost-effective upgrade for any application that uses Intel 80C186 family of products or any other code-compatible 16-bit microprocessors.

The Intel386 EX embedded processor, which is an enhanced Intel386 SX processor with integrated PC-AT and embedded peripherals, offers the designer higher performance for implementing real-time functions and sophisticated user interfaces. Shorter bus cycles, an internal 32-bit architecture, a demultiplexed bus, and address pipelining result in a much higher performance than the 80C186.

All of the functions integrated onto the 80C186 family are maintained on the Intel386 EX embedded processor. The Intel386 EX embedded processor peripherals are designed to be compatible with PC peripherals. Having PC compatible peripherals is a significant benefit. DOS is a well-understood operating system with over 50,000 existing applications. DOS also has the benefit of rapid code development for an application. To stay competitive in the embedded market, short product development cycles are critical. The Intel386 EX embedded processor will run DOS applications much more efficiently than the 80C186 family.

With embedded designs becoming more sophisticated, the code requirements have increased beyond the I Mbyte capability of the 80C186 family. Intel386 EX embedded processor has a 26-bit address bus (enhanced from the 24-bit Intel386 SX processor bus), providing a 64 Mbyte address space.

The instruction set of the Intel386 EX embedded processor is a superset of the 80C186 and maintains 100% object code compatible with the 80C186. Code written for the 80C186 will execute on the Intel386 EX embedded processor without any modification, but developers can take advantage of the 32-bit instructions to maximize performance.

This application note will look at all the integrated peripherals of the Intel386 EX embedded processor and discuss how they meet and/or enhance the functionality of the 80C186 family peripheral functions.

2.0 80C186 FAMILY AND Intel386 EX EMBEDDED PROCESSOR ARCHITECTURE

The 80C186 family represents the third generation addition to Intel's 80186 family of embedded microprocessors. Intel's advanced CHMOS IV semiconductor fabrication technology has allowed the integration of many of today's most used peripherals with a high performance, low-power, 8086 compatible CPU core. The 80C186 family has a new and enhanced feature set that includes:

- Power/Static CMOS Modular CPU Core
- Power Management Unit
- Serial Communication Unit
- Input/Output Unit
- Enhanced Chip Select Unit
- Refresh Control Unit
- Interrupt Control Unit
- Timer/Counter Unit
- Direct Memory Access Unit
- Watchdog Timer

The 80C186 family CPU core shares the same instruction set as the 8086/8088 while adding some new instructions. The 80C186 family is supported by a wide variety of programming solutions provided by third party vendors. For enhanced floating point performance, the 80C186 family provides interfacing support to the 80C187 Numerics Processor.

The Intel386 EX embedded processor is a highly integrated Intel386 CPU core-based processor that has been optimized for embedded applications. It has a modular, fully static Intel386 SX CPU core with an enhanced power management capability using the Intel System Management Mode (SMM).

The Intel386 EX embedded processor can address up to 64 Mbytes (26-bit address bus) of physical memory and up to 64Kbytes of I/O. It also supports pipelining, which allows for high bandwidth with relatively slow and inexpensive components. A 16-bit external data bus has been implemented in order to simplify system design and minimize the memory component count.

The *Intel386* EX embedded *processor supports* an *enhanced feature set that includes the following:*

- Static CMOS Modular CPU Core
- Clock generation and Power Management Unit
- System Management Mode
- Programmable Chip Select unit
- DMA unit
- Timer/Counter unit
- Interrupt Controller unit
- *Asynchronous SIO unit*
- Synchronous SIO unit
- DRAM/PSRAM Refresh unit
- Watchdog Timer unit
- JTAG Boundary Scan
- Parallel I/O unit

Table 2-1 gives the reader a quick look at the peripherals available on the 80C186 family and the Intel386 EX embedded processor.

Table 2-1. Comparison of 80C186 Family and Intel386 EX Embedded Processor

Feature	80C186XL	80C186EA	80C186EB	80C186EC	Intel386™ EX CPU
Enhanced 8086 Instruction Set					
Low Power Static Modular CPU					Intel386 SX CPU
Power Save(Clock Divide) Mode					
Powerdown and Idle Modes					
80C187 Interface					Intel387™ SX coprocessor
ONCE Mode					
Interrupt Control Unit					
Timer/Counter Unit	3 16-bit	3 16-bit	3 16-bit	3 16-bit	3 16-bit
Chip-Select Unit	13 Channels	13 Channels	10 Channels	10 Channels	8 Channels
DMA Unit	2 Channels	2 Channels		4 Channels	2 Channels
Serial Communication Unit					
Refresh Control Unit					
Watchdog Timer Unit					
I/O Ports			16 Total	22 Total	24 Total
SMM					
JTAG					

3.0 BUS INTERFACE UNIT

The Intel386 EX embedded processor's Bus Interface Unit (BIU) provides the same functionality as the 80C186 family of microprocessors. The BIU generates bus cycles that prefetch instructions from memory, pass data to and from the execution unit, and pass data to and from the integrated peripherals. The Intel386 EX embedded processor defines a bus cycle with address, data, status, and control information driven by the BIU. Bus hold, interrupt acknowledge, refresh, and lock cycles are also managed by the BIU. In addition to supporting the 80C186 features, the Intel386 EX embedded processor BIU has many enhancements and new features.

3.1 Intel386 EX Embedded Processor BIU Enhancements

- De-multiplexed address and data bus
- 2 clock bus cycles (8-bits/clock throughput)
- Improved 8-bit transfer management
- Pipelining

3.2 Bus Cycles

The Intel386 EX embedded processor's bus cycles are very similar to the 80C186. The start of a bus cycle presents the address of the memory or I/O location and status information defining the type of bus cycle. Read or write control signals follow the address and define the direction of data flow. The bus cycle is completed and terminated by the READY X signal.

The Intel386 EX embedded processor can complete a bus cycle in two clocks compared to the 80C186 microprocessor's four clocks.

3.3 Clock Cycles

The Intel386 EX embedded processor uses a double-frequency clock input (CLK2). This clock is internally divided by two and synchronized to the falling edge of RESET to generate the internal processor clock signal. Each processor clock cycle is two CLK2 cycles wide with each CLK2 cycle defining a phase of the processor clock.

3.4 De-Multiplexed Address and Data Bus

To reduce the complexity and volume of external logic, the Intel386 EX embedded processor does not implement a time-multiplexed bus as does the 80C186 (see Table 3-1). Because the address and data bus signals are driven on separate pins, they do not have to be latched externally. Consequently, the address latch enable (ALE), Data Transmit or Receive (DT/R#), and the Data Enable (DENX) signals are not needed or provided by the Intel386 EX embedded processor. Instead of latching the bus definition on the ALE signal, the Address Strobe Signal (ADSX) indicates the beginning of a non-idle bus cycle.

Table **3-1.** Address and Data Bus Signals

	Intel386™ EX Embedded Processor	80C186 Microprocessors
Address Bus	A25:1, BLE#	A19:16, AD15:0
Data Bus	D15:0	AD15:0
Byte High Enable	BHEX	BHE#
Address Status	ADS#	ALE
Data Latch Signals		DT/R#, DEN#

The Intel386 EX embedded processor represents the least significant address bit (A0 on the 80C186) with the Byte Low Enable (BLEX) signal. The BLEX signal is used in conjunction with the Byte High Enable (BHEX) signal to easily implement bank memory subsystems. See Table 3-2 below.

Table 3-2. Byte and Word Transfer Signals

	Intel386™ EX Embedded Processor		80C186 Microprocessor	
	BHE#	BLE#	BHE#	A0
Word transfer	0	0	0	0
Upper byte transfer	0	1	0	1
Lower byte transfer	1	0	1	0
Refresh transfer	1	1	1	1

3.5 Bus Cycle Types

The Intel386™ EX embedded processor supports the same 80C186 status and control signals (see Table 3- 3).

Table 3-3. Status and Control Signals

Intel386™ EX Embedded Processor	80C186 Microprocessors
M/IO#, D/C#, W/R#	S2:0#
WR#	WR#
RD#	RD#
LOCK#	LOCK#
HOLD	HOLD
HLDA	HLDA

Both the 80C186 and the Intel386 EX embedded processor have three status signals that define the processor's bus cycles. Table 3-4 lists the differences between the two processor's status signals. An Intel386 EX embedded processor idle cycle is indicated by the absence of ADS# active.

Table 3-4. Bus Cycle Types

	Intel386™ EX Embedded Processor			80C186 Micro-processors		
	M/IO#	D/C#	W/R#	S2#	S1#	S0#
Interrupt Acknowledge	0	0	0	0	0	0
I/O Read	0	1	0	0	0	1
I/O Write	0	1	1	0	1	0
Halt	1	0	1	0	1	1
Instruction Prefetch	1	0	0	1	0	0
Memory Read	1	1	0	1	0	1
Memory Write	1	1	1	1	1	0
Idle	X	X	X	1	1	1

3.5.1 Refresh Cycles

In addition to the 80C186-like status signals, the Intel386 EX embedded processor provides a separate REFRESH# status pin. An Intel386 EX embedded processor refresh cycle is defined by the same status signals as a "memory read cycle" with the REFRESH# signal active. But, like the 80C186, BHE# and BLE# inactive also indicates a refresh cycle.

3.5.2 Interrupt Acknowledge Cycles

The Intel386 EX embedded processor's interrupt control unit consists of two cascaded 8259A interrupt controllers. Consequently, the interrupt acknowledge cycles are defined to work in conjunction with 8259A. See the ***Intel386™ Embedded Microprocessor Hardware Reference*** (Order Number 272485) for more details on the interrupt acknowledge cycle.

3.5.3 Pipelined Bus Cycles

The Intel386 EX embedded processor provides pipeline bus cycles to implement a fast memory system with slower memory devices. Pipeline bus cycles provide the next bus cycle address during the current bus cycle. This gives slower memory an extra cycle to access the correct memory locations. See the ***Intel386™ Embedded Microprocessor Hardware Reference*** (Order Number 272485) for more details on pipelined bus cycles.

3.6 Wait States and Ready Generation

The READY# signal completes and terminates each bus cycle on the Intel386 EX embedded processor and can be driven by external logic or the chip-select unit. During on-chip peripheral accesses, the BIU still drives the address on the bus. If external memory or logic is mapped to the same address as an on-chip peripheral, the READY# signal can be qualified with the Local Bus Access (LBA#) signal. The LBA# signal is active when the processor accesses an internal peripheral or when the chip-select unit provides the READY# signal.

3.7 8-/16-Bit Transfer Cycles

One of the Intel386 EX embedded processor BIU enhancements is the Bus Size (BS8#) signal. The BS8# control signal allows the external logic to dynamically switch between an 8-bit data bus size and a 16-bit data bus size. In addition, the Intel386 EX embedded processor's chip-selects can be programmed to automatically assert the BS8# signal.

4.0 PERIPHERAL CONTROL REGISTERS/CHIP CONFIGURATION

Both the Intel386 EX embedded processor and the 80C186 processors access their integrated peripherals through a number of peripheral control registers. The functions of the peripheral control registers on the 80C186 processors are fully supported by the Intel386 EX embedded processor. In addition, the Intel386 EX embedded processor has introduced some new registers to support its PC/AT compatible peripherals. Numerous configuration registers exist on the Intel386 EX embedded processor to support the mutliplexing scheme implemented on the processor.

4.1 Addressing of the Peripheral Registers

Like the 80C186 processors, the peripheral registers on the Intel386 EX embedded processor are located in contiguous bytes in memory. However, while the peripheral control registers on the 80C186 are addressed at fixed offsets in a relocatable 256-byte Peripheral Control Block (PCB), those on the Intel386 EX embedded processor are only accessible in one of two possible fixed address locations (see Table 4-1). These are contained in the I/O space and the DOS I/O space.

Table 4-1. Valid Address Locations tor the Peripheral Registers

	Intel386 EX Processor	80C186 Processors
Memory space	Not available	Any 256-byte boundary
I/O space	Reside physically in I/O space (address 0F000H-0F8FFH) May be mapped into DOS I/O space (addresses 0H-03FFH)	Any 256-byte boundary

4.2 Intel386 EX Embedded Processor Peripheral

The peripheral control registers on the Intel386 EX embedded processor are addressable through either the 1/0 space or the DOS I/O space. Four addressing modes exist including DOS-compatible, Nonintrusive DOS, Enhanced DOS, and Non-DOS. Non-DOS mode corresponds to the operation of the 80C186 processors (see Table 4-2). Using the other modes will enable the system design to become PC/AT- compatible.

Table 4-2. Peripheral Addressing Modes

	DOS-Compatible	NonIntrusive DOS	Enhanced DOS	Non-DOS
Expanded I/O space	Disabled	Disabled	Specific PC/AT-compatible peripherals are accessible All other peripherals are accessible	All peripherals are accessible
DOS I/O space (mapped)	All PC/AT-compatible peripherals are accessible	Specific PC/AT-compatible peripherals are accesible	Specific PC/AT-compatible peripherals are accessible	No peripherals are accessible

Table 4-3. Programming the Relocation or Configuration Register

80C186: PCB Relocation Register (RELREG)	Intel386 EX Processor: Address Configuration Register (REMAPCFG)
• Located at a fixed offset within the PCB.	• Located at I/O address 22H and 23H.
• Programs the PCB base address.	• Enables or disables the I/O space. Controls which I/O space the peripherals are addressable in. Selects the peripheral addressing mode.
• At reset, the PCB base address is programmed for the top of I/O address space (address FFOOH).	• At reset, all PC/AT-compatible peripherals are mapped into and accessible from DOS I/O space

4.3 Programming the Address of the Peripheral Registers

Both the 80C186 processors and the Intel386 EX embedded processor have a single register which is used to control the addressing of the peripheral control registers. The control registers of the two processor families are summarized in Table 4-3.

4.4 Enabling the Expanded I/O Space

Using the Intel386 EX embedded processor in traditional embedded applications invariably requires the use of certain peripherals in the expanded I/O space. However, this space is disabled at reset. The following code must be written in order to enable the expanded I/O space:

```
MOV   AX, 8000H    ;
OUT   23, AL       ; write COH to 23H
XCH   AL, AH
OUT   22, AL       ; write 80H to 22H
OUT   22. AX       ; write 0080H to 22H
```

Once this is done, the Address Configuration Register (REMAPCFG) is writeable, and the PC/AT-compatible peripherals are accessible in either the expanded or the DOS I/O space. All other peripherals are accessible through the expanded I/O space.

4.5 Chip Configuration

The Intel386 EX embedded processor is a heavily multiplexed device. One must be careful in configuring the device, making sure that two peripherals sharing a multiplexed device pin are not both used. For more information, see the ***Intel386™ EX Embedded Microprocessor Hardware Reference*** (Order Number 272485).

5.0 CLOCK AND POWER MANAGEMENT UNIT

The Intel386 EX embedded processor's clock and power management unit supports most of the functionality available on the 80C186 processors. Both processor families support idle and powerdown modes and a divide-by-two circuit. Some differences and/or enhancements exist on the Intel386 EX embedded processor which are summarized as follows:

- The Intel386 EX embedded processor does not support an on-chip oscillator. It must use a "canned oscillator".
- The Intel386 EX embedded processor generates two additional clock signals in addition to the processor clock: SERCLK and PSCLK. These clocks are routed to certain integrated peripherals. They are not supported by the 80C186 processors.
- Power save mode is not supported by the Intel386 EX embedded processor.
- The Intel386 EX embedded processor supports System Management Mode (SMM), which is used to implement system wide power management.

5.1 Clock Generation Circuitry

5.1.1 Oscillator

Unlike the 80C186 processors, the Intel386 EX embedded processor does not provide the option of using an on-chip oscillator. A "canned oscillator" must be used, as is done on 80C186 processor designs which do not use the internal oscillator. The external clock generated by the canned oscillator is input to the device through the CLK2 device pin on the i386 processor and the CLKIN device pin on the 80C186 processors. This clock provides the fundamental timing for the processor.

5.1.2 Generated Clock Signals

As is done on the 80C186 processors, the external clock input to the Intel386 EX embedded processor is modified by a divide-by-two circuit to generate a 50% duty cycle clock signal. The processor clock is thus $CLK2/_2$ for the Intel386 EX embedded processor, corresponding to the processor clock of $CLKIN/_2$ for the 80C186 processors. On the 80C186 processors, this processor clock is available as an output through the CLKOUT device pin. The Intel386 EX embedded processor does not provide a processor clock output pin, therefore external devices must be used to generate their own divide-by-two.

The Intel386 EX embedded processor is enhanced to generate two other clock signals in addition to the processor clock signal: SERCLK and PSCLK. A second divide-by-two counter is used to generate the SERCLK signal, whose frequency is equal to $CLK2/_4$. This clock signal is routed to the asynchronous and synchronous serial I/O units.

The second additional clock signal, PSCLK, is generated through the use of programmable divider circuitry. PSCLK is generated by dividing the processor clock by an offset of the value written to the Clock Prescale Register. The possible internal frequency of PSCLK ranges from $CLK2/_4$ to $CLK2/_{1026}$. The PSCLK signal is routed to the synchronous serial I/O unit and the timer/counter unit.

5.1.3 Power Management Circuitry

The Intel386 EX embedded processor supports a PWRDOWN signal which is available through a device pin. This signals that the processor has entered powerdown mode. External logic can use this signal to implement system wide power management. This signal is not available on the 80C186 family.

5.2 Power Management Modes

Like the 80C186 processors, the Intel386 EX embedded processor is in active mode after being reset. In this mode, the clock signal is routed to the CPU and the integrated peripherals, and power consumption is at a maximum. Both the 80C186 processors and the Intel386 EX embedded processor offer certain power management modes which may be entered in order to reduce power consumption. A summary of the available power management modes is shown in Table 5-1.

System management mode (SMM) allows the execution of system-wide routines that are independent and transparent to the operating system. SMM interacts with the available power management modes, and it is entered whenever a system management mode interrupt (SMI#) is received.

Table 5-1. Available Power Management Modes

	Intel386 EX Processsor	80C186EC	80C186EB	80C186EA	80C186XL
Active					
Idle					
Power Save					
Powerdown					
SMM					

Table 5-2. Comparison of Power Management Modes

	Active	Idle	Power Save	Powerdown
CPU clock	operating	Stopped	operating at programmed clock frequency	Stopped
Peripheral clock	operating	operating	operating at programmed clock frequency; peripherals may need to be reprogrammed to compensate for overall reduced clock rate	Stopped
CLKOUT (80C186 only)	operating	operating	operating at programmed clock frequency	Stopped
Relative Power	Full	Low	Adjustable	Lowest
User Overhead	—	Low	Moderate to High	Low to Moderate
Chief Advantage	full-speed	peripherals are unaffected	code execution continues	long battery life

5.3 Programming the Clock and Power Management Unit

The registers used to program the clock and power management unit on the Intel386 EX processor are slightly different from those used on the 80C186 processors. The differences involve the deletion of one of the registers used by the 80C186 processors, and the addition of a register. The Power Save Register used in the 80C186 processors is not used in the Intel386 EX processor, since it does not support power save mode. Also, the Clock Prescale Register is needed to support the enhancement of routing a prescaled clock to some of the integrated peripherals. A description of the registers used by the Clock and Power Management Unit on the Intel386 EX processor is found below.

Power Control Register	Controls whether the processor enters idle or powerdown mode.
Clock Prescale Register	Determines the divisor used to generate the frequency of PSCLK. Legal values are from 000H (divide by 2) to 01FFH (divide by 513), with the divisor equal to the written value plus 2.

5.4 Entering and Exiting Power Management Modes

The Intel386 EX processor enters a power management mode by programming the power control register and then executing a HALT instruction, just as the 80C186 processors do. The power management mode is exited and the device returns to active mode if an NMI, unmasked interrupt, system management interrupt (SMI#), or a reset occurs. The processor will reenter the power management mode when the next HALT instruction is executed.

5.5 BIU operation during Power Management Modes

In idle mode, the core clocks are temporarily turned on so that the BIU is able to handle DMA, refresh, and hold requests. These requests are unable to be processed during powerdown mode.

6.0 INTERRUPT CONTROL UNIT

The Interrupt Control unit (ICU) on the Intel386 EX embedded processor is identical to the ICU on the 80C186EC. Both are functionally identical to two industry-standard 82C59As connected in cascade. The system designer, bearing in mind pin multiplexing and the connections of internal and external interrupt sources, should be able to port his 80C186EC code as is to the Intel386 EX embedded processor.

The ICUs of the 80C186XL/EA/EB are not based on the industry standard 82C59As, hence some upgrades are required to port the ICU code to the ICU of the Intel386 EX embedded processor.

6.1 Intel386 EX Embedded F Interrupt Control Unit e s/ Enhancements

The Intel386 EX embedded processor and the 80C186EC ICUs are composed of two 82C59As modules connected in cascade. Functionally, both units are compatible. However, the implementation of the connections of the interrupt sources are different. This is due to the mix of peripherals and capabilities implemeted on the Intel386 EX embedded processor and the 80C186EC.

- Both processors support single maskable interrupt input to the CPU.
- Both processors supports 8 external interrupts. The Intel386 EX embedded processor supports one more internal interrupt than the 80C186EC (8 total).
- Both processors support the same interrupt priority scheme.
- Both processors support the same interrupt modes.
- The implementation of interrupt masking is identical on both processors.
- The Intel386 EX embedded processor supports cascading with up to 4 other 82C59 modules (7 on the 80C186EC).

6.2 Intel386 EX Embedded or t C i t U Operation

The Intel386 EX embedded processor CPU core, like the modular core of the 80C186EC, supports a single maskable interrupt input. The single interrupt input capability is expanded through the implementaion of an interrupt controller. This controller acts like a filter between the multiple interrupt request inputs and the the single interrupt request to the CPU. The following sections will discuss the interrupts sources, priority, modes, masking, and cascading supported by the interrupt controller.

6.2.1 Interrupt Sources

The master and slave modules of the Intel386 EX embedded processor and the 80C186EC control different interruot sources. Tables 6-1 and 6-2 list the interruot sources for the Intel386 EX embedded processor and the 80C186EC in master and slave modes.

Table 6-1. Master Mode Interrupt Sources

Master Mode	Intel386™ EX Processor	80C186EC
IR0	Timer output	External Interrupt, INTO
IR1	External Interrupt, INTO	External Interrupt, INTI
IR2	Slave 8259A cascade	External Interrupt, INT2
IR3	Serial IO interrupt 1	External Interrupt, INT3
IR4	Serial IO interrupt 0	External Interrupt, INT4
IR5	External Interrupt, INTI	External Interrupt, INT5
IR6	External Interrupt, INT2	External Interrupt, INT6
IR7	External Interrupt, INT3	Slave 8259A cascade

Table 6-2. Slave Mode Interrupt Sources

Slave Mode	Intel386™ EX Processor	80C186EC
IR0	External Interrupt, INT4	Timer 0 Maximum Count
IR1	Synchronous SIO interrupt or INT5	Timer 1 Maximum Count
IR2	Timer output 1	DMA Channel 2 terminal count
IR3	Timer output 2	DMA Channel 3 terminal count
IR4	DMA interrupt	Timer 2 Maximum Count
IR5	External Interrupt INT6	Serial channel 0 receive complete
IR6	External Interrupt, INT7	Serial channel 0 transmit complete
IR7	Watchdog timer output	External interrupt, INT7

Table 6-3 lists the number of interrupt sources available to the Intel386 EX embedded processor and the 80C186 family.

6.2.2 Interrupt Priority and Nesting

Since both the Intel386 EX embedded processor and the 80C186EC are composed of 8259A modules, the prioritization scheme or the interrupt structure is the same. After initialization, the 8259A module sets the priorities of the interrupt levels to the default condition, in which IR7 is the lowest priority and IRO is the lowest.

Since some systems may require the alteration of default priority during program execution, both the Intel386 EX embedded processor and the 80C186EC support specific and automatic rotation.

In specific rotation mode, you can reprogram any of the IR lines to be the lowest-priority interrupt source. The priorities of the remaining IR lines are then redefined in a circular fashion. Figure 7-1 illustrates the priority rotation of interrupts.

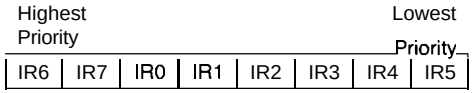

Figure 7-1. Specific Rotation

In automatic rotation mode, an IR line is automatically assigned the lowest priority after the service routine for that interrupt has been completed. The respective priorities of the other pending interrupts are changed in the same circular fashion described above.

Both the Intel386 EX embedded processor and the 80C186EC support the same nesting struture. Fully nested, special-fully nested, special mask, and poll command modes are supported by both the embedded processors. Table 6-4 compares the nesting structure of the various embedded processors.

6.2.3 Interrupt Requests

The processing of an external interrupt is the same on both the Intel386 EX embedded processor and the 80C186EC. It begins with assertion of an interrupt request signal on one of the IR lines. This signal goes through the edge/level detection circuitry, which they both support, and then moves to the Interrupt Request Register.

6.2.4 Interrupt Masking

All Intel embedded processors support enabling or disabling of the external maskable interrupts globally. This is achieved by setting or clearing the Interrupt Enable Flag bit in the Processor Status Word register. The interrupt sources can also be individually enabled or disabled using the Interrupt Mask register.

Table 6-3. Number of Interrupt Sources

	80C186EA	80C186XL	80C186EB	80C186EC	Intel386™ EX CPU
Internal	5	5	5	7	8
External	4	4	5	8	8
Cascade	Yes	Yes	Yes	Yes	Yes

Table 6-4. Interrupt Nesting

	80C186EA	80C186XL	80C186EB	80C186EC	Intel386™ EX CPU
No nesting	Yes	Yes	Yes	No	No
Fully nested	Yes	Yes	Yes	Yes	Yes
Special-fully nested	Yes	Yes	Yes	Yes	Yes
Poll command	Yes	Yes	Yes	Yes	Yes
Special mask	Yes	Yes	Yes	Yes	Yes

6.2.5 Interrupt Cascading

With 4 external interrupts connected to the master module, the Intel386 EX embedded processor is able to cascade up to 4 other slave 8259A modules. The 80C186EC master module, on the other hand, can cascade up to 8 slave interrupt controllers. This can extend the interrupt request capability, in a fully cascaded system, to 64 levels on the 80C186EC.

The 80C186XL/EA/EB can cascade with up to 2 slave 8259A modules.

6.3 Programming the ICU of the Intel386 EX Embedded Processor

With the ICU of the Intel386 EX embedded processor being the same as the 80C186EC, the system designer should be able to port his 80C186EC code as is to the Intel386 EX embedded processor. The designer, however, must pay special attention to the pin configuration registers and configure the interrupt sources properly. Also, three 80C186EC registers, namely the interrupt request latch registers, are not supported on the Intel386 EX embedded processor because there is no need to. The pending bit of an interrupt request, is not cleared until the interrupt is serviced or you read the interrupt request register.

Table 6-5 lists the ICU registers for both the Intel386 EX embedded processor and the 80C186EC.

Table 6-5. Interrupt Registers

Register Name	Register Function	80C186EC	Intel386™ EX CPU
Port 3 configuration register	Det. which signals are connected to package pins	N/A	Yes
Interrupt configuration register	Determines the slave's IR signal connections	N/A	Yes
Init Comm. Word. ICWI	Begins 8259A initialization sequence	Yes	Yes
Init Comm. Word, ICW2	Sets the base interrupt type for the module	Yes	Yes
Init Comm. Word, ICW3, master	Selects cascaded input pins on master	Yes	Yes
Init Comm. Word, ICW3, slave	Sets slave ID for slave 8259A moule	Yes	Yes
Init Comm. Word, ICW4	Selects SFN mode and AEOI mode	Yes	Yes
Oper Comm. Word OCWI	Interrupt mask register	Yes	Yes
Oper Comm. Word OCW2	Priority and EOI commands	Yes	Yes
Oper Comm. Word OCW3	Controls special mask mode and register reading	Yes	Yes
Inter Req Reg.	Indicates pending interrupt request	Yes	Yes
In-service register	Indicates request that are being serviced	Yes	Yes
Poll status byte register	Ind. if any device connected to 8259A require servicing	Yes	Yes
DMA interrupt request latch	Latches DMA interrupt request	Yes	N/A
Serial interrupt request latch	Latches serial interrupt request	Yes	N/A
Timer interrupt request latch	Latches timer/counter interrupt request	Yes	N/A

7.0 Timer and Counter Unit

Both the 80C186 family's Timer Counter Unit (TCU) and the Intel386 EX embedded processor's TCU contain logic and three independent 16-bit down counters. These counters can be driven by a prescaled value of the processor clock or an external device. The counter's output signals can appear at device pins, generate interrupt requests, and initiate DMA transactions. With the exception of dual maximum mode, all the 80C186 family TCU functions can be implemented with the Intel386 EX embedded processor's DMA controller.

7.1 Intel386 EX Embedded Processor TCU Enhancements/Features

The TCU on the Intel386 EX embedded processor is a superset of the 80C186 family TCU.

- Upon reset, much like the 80C186 family, the contents of the count registers are indeterminate and they should be initialized to zero before any timer operation.
- Supports binary and BCD count format (80C186 family support binary format only).
- All three timer inputs can be clocked internally and externally. This is limited to two timers on the 80C186.
- Timer inputs can be configured to be tied internally to V_{CC}. On the 80C186 family, this must be done externally. This is to support continous counting mode.
- Intel386 EX embedded processor's embedded processor supports six different counting modes. This allows the system designer to implement all the 80C186 TCU functions with the exception of dual maximum mode.

7.2 TCU Operation

7.2.1 Count Format

The Intel386 EX embedded processor TCU supports the binary count format of the 80C186 and the BCD count format. The counters decrement (80C186 counters increment) on the rising edge of clock. The highest count value is 0FFFFH for binary counting or 9999 for BCD counting. To specify the count format, write to the timer control register's control word format, TMRCON.

7.2.2 Clocking

The TCU on the Intel386 EX processor, much like the one on the 80C186 family can be configured to be clocked internally or externally. To configure the Intel386 EX processor timers for internal or external clocking, write to the timer configuration register, TMRCFG.

For internal clocking, the Intel386 EX processor TCU timers, TO. T1. and T2 can be clocked internally by a prescaled clock signal (PSCLK) up to 1/4 CLK2 frequency. CLK2 is the internal clock frequency on the Intel386 EX processor.

For external clocking, T0, T1 of the 80C186 family and all three timers of the Intel386 EX processor can be clocked externally at up to 1/4 of the internal clock frequency.

7.2.3 Inputs/Outputs

Each counter's GATEn signal on the Intel386 EX processor can be connected to either its timer gate (TMRGATEn) pin or V_{CC}. The timer configuration register (TMRCFG) can be configured to enable the GATEn signal connections. On the 80C186 family, the Vcc signal connection is not available and must be wired externally (this will enable timers at all times).

Each counter's GATEn signal affects its counting operation. Table 7-1 shows the operations caused by GATEn:

Table 7-1. i386 EX Processor Counter GATEn Signal Effects

Count Mode	Gate-trigger	Low-level on GATEn	High-level on GATEn
0 and 4	—	Disables or suspends counting	Enables or resumes counting
1 and 5	Loads count value	—	—
2 and 3	Loads count value	Disables or suspends counting	Enables or resumes counting

Each counter's OUTn signal on the Intel386 EX processor can be connected to either its timer out (TMROUTn) pin or to the interrupt control unit (counter 1 and 2). At reset, the output signal (OUT1) is connected to DMA channel 0, and counter's 2 output signal (OUT2) is connected to DMA channel 1.

7.2.4 Counting Modes

Each counter on the Intel386 EX processor supports six different counting modes. Table 7-2 discusses these modes and how they meet the functionality of the 80C186 family counting modes:

Table 7-2. i386 EX Processor TCU Counting Modes

Mode	Mode Description	Mode Functions	Similar 80C186 family Function
Mode 0	Interrupt on terminal count	GATEn is level sensitive OUTn is reset when initialized Count loaded on CLKINn pulse after a count write OUTn is set on terminal count Counter rolls to highest count	Supports single maximum mode
Mode 1	Hardware retriggable one-shot	GATEn is edge sensitive OUTn is set when initialized Count loaded and OUTn reset after gate trigger OUTn set on terminal count Counter rolls to highest count	Supports single maximum mode
Mode 2	Rate generator	GATEn is level/edge sensitive OUTn is set when counter initialized Count loaded on CLKINn pulse after a count write Count loaded on terminal count or gate trigger OUTn reset for one cycle when count reaches one Periodic mode	Supports single maximum continous mode
Mode 3	Square Wave	GATEn is level/edge sensitive OUTn is set when initialized Counter decrements by 2 on each CLKINn pulse Periodic mode	Supports single maximum mode Supports varied duty cycles
Mode 4	Software-triggered strobe	GATEn is level sensitive OUTn is set when initialized Count loaded on CLKINn pulse after a count write OUTn reset on terminal count and set on next CLKINn pulse Counter rolls to highest count	Supports single maximum mode
Mode 5	Hardware-triggered strobe	GATEn edge sensitive OUTn is set when initialized Gate trigger required to load count OUTn reset on terminal count and set on next CLKINn pulse Counter rolls to highest count	Supports single maximum mode

7.2 Programming the TCU

Different configuration options are available on the TCU of the Intel386 EX processor. Three configuration registers, TMRCFG, P3CFG, and PINCFG are provided in order to specify the connections of the input/output signals on the TCU. These registers are not applicable to the TCU of the 80C186 family. See Table 7-3 for the TCU registers.

Using the three configuration registers along with the timer control and counter registers of the Intel386 EX processor, the designer can support all functions supported by the timer control and count registers of the 80C186 family except for the ALTernate compare register function. The TCU of the 80C186 family includes two compare registers to support dual maximum mode. This mode is not supported by the Intel386 EX processor.

Unlike the 80C186, you can write a value directly to a counter on the Intel386 EX processor. However, the 16-bit counters are read and written a byte at a time. The control word format of TMRCON selects whether you read or write the LSB only, MSB only, or LSB then MSB.

8.0 WATCHDOG TIMER UNIT

The Intel386 EX embedded processor's watchdog timer unit is a superset of the WDT unit available on the 80C186EC. It can function as a system watchdog or a general-purpose timer. Bus monitor mode which was not implemented on the 80C186EC is available on the Intel386 EX embedded processor.

8.1 Intel386 EX Embedded Processor Watchdog Timer Unit Enhancements/Features

The Intel386 EX embedded processor's watchdog timer unit supports the same features as the 80C186EC, but is more enhanced:

- The LOCKed instruction sequence is executed by writing two sequential words to the WDTCLR location. On the 80C186EC two sequential bytes are written to the WDTCLR location.
- When the WDT times out, an 8-state binary counter drives the WDTOUT pin high for eight clock cycles. On the 80C186EC, the WDTOUTX pin is driven low for 4 clock cycles. The WDTOUT signal pin is an active high signal, whereas on the 80C186EC, it is an active low signal.
- An internal signal carries the inverted value of WDTOUT pin on the Intel386 EX embedded processor to the interrupt control unit (the slave's IR7 line). On the 80C186EC, you have to tie the WDTOUTX pin externally to one of the INTx pins through an inverter.
- The WDT is disabled by setting the CLKDIS bit in the WDT STATUS register. On the 80C186EC, the WDT is disabled when a LOCKed instruction sequence is executed.
- Bus monitor mode is not supported on the 80C186EC.

Table 7-3. TCU Registers

Register Name	Intel386™ EX Processor	80C186 Family
Timer configuration register	TMRCFG	N/A
Port 3 configuration register	P3CFG	N/A
Pin configuration register	PINCFG	N/A
Timer control register	TMRCON--Control word format Counter-latch format Read-back format	TnCON
Timer counter register	TMRn---Write, read, and status	TnCNT
Timer compare A register	N/A	TnCMPA
Timer compare B register	N/A	TnCMPB

8.2 Watchdog Timer Operation

Both the 80C186EC and the Intel386 EX embedded processor WDT units operate in the same manner where after device reset, the WDT begins counting down in general-purpose timer mode. Unless the designer changes the mode, changes the reload value, or disables it, the WDT will time out and assert WDTOUT after 64K clock cycles. The 32-bit down counter decrements on every clock cycle.

8.2.1 System Watchdog

Using the WDT as a system watchdog allows the system to recover from a software upset. This can be achieved through either a full system reset or an interrupt request. For a full system reset, the power-on reset signal and the WDTOUT (WDTOUT# on the 80C186EC) signal must be ANDed together to produce the RESET (RESIN# on the 80C186EC) signal for the processor. To use the WDT to interrupt the processor, one can tie the WDTOUT# directly to the INTx pin (on the Intel386 EX embedded processor, it is tied internally), or to the NMI pin through an inverter. The interrupt control unit must be programmed for edge sensitivity.

In system watchdog mode, the software must periodically reload the down-counter with the reload value, so the 32-bit down counter never reaches zero.

To enable the WDT unit on both processor families as a system watchdog, the following sequence must be followed:

- Write the upper 16 bits of the reload value to WDTRLDH
- Write the lower 16 bits of the reload value to WDTRLDL
- Execute the appropriate LOCKed instruction sequence to reload the down counter and lock accesses to the WDT reload value.
  - — On the Intel386 EX embedded processor, you have to write two sequential words, 0F01EH followed by OFEIH, to the WDTCLR location.
  - — On the 80C186EC, you have to write two sequential bytes, OAAH followed by 55H, to the WDTCLR location.

8.2.2 General-Purpose Timer

The WDT defaults to general-purpose timer mode after reset. Beginning at OFFFFH at reset, the down counter begins decrementing once every clock cycle and times out when it reaches zero. Once it times out, an 8-state binary counter on the Intel386 EX embedded processor drives the WDTOUT pin high for eight clock cycles. On the 80C186EC, the WDTOUT# pin is driven low for 4 clock cycles. During the clock cycle immediately after the down counter reaches zero, this mode reloads the down counter with the contents of the reload registers. Reprogramming of the WDT reload register is allowed in this mode since the LOCKed sequence was not executed.

8.2.3 Bus Monitor Mode

This mode is only available on the Intel386 EX embedded processor. It can be enabled by writing a 32-bit value to the WDTRLDH and WDTRLDL registers, using two word writes, and then setting the bus monitor bit in the WDTSTATUS register. Unlike the general-purpose mode, where you can only reload the down counter on a WDT timeout, the bus monitor mode allows you to change the reload value and enable or disable the mode at any time.

8.3 Programming the Watchdog Timer

8.3.1 Register Mnemonics

Six Peripheral Control Block registers control the WDT unit on the 80C186EC and the Intel386 EX embedded processor. Table 8-1 summarizes these registers and their functions.

Table 8-1. WDT Registers

Register Name	Intel386™ EX Processor	80C186EC
WDTRLDH	WDT reload high	Same
WDTRLDL	WDT reload low	Same
WDTCNTH	WDT count high	Same
WDTCNTL	WDT count low	Same
WDTCLR	WDT clear	Same
WDTDIS	N/A	WDT disable
WDTSTATUS	WDT status; You can disable WDT by setting the CLKDIS bit	N/A

8.3.2 Reloading the Watchdog Timer

Like the 80C186EC, the reload registers on the Intel386 EX embedded processor hold a user-defined value that reloads the down counter when the system software executes a LOCKed sequence in watchdog mode or the down-counter reaches zero in general-purpose timer mode. In addition, in bus monitor mode on the Intel386 EX embedded processor, the reload registers are reloaded when the bus interface unit asserts ADS#

8.3.3 Disabling the Watchdog Timer

On the 80C186EC, the WDT is disabled when a LOCKed instruction sequence is executed. A sequential write of two bytes to the WDTDIS register, 55H followed by OAAH, written by a single LOCKed instruction, will disable the WDT. The WDT on the 80C186EC can not be disabled once it has been reloaded by the system software.

On the Intel386 EX embedded processor, the WDT is disabled by setting the CLKDIS bit in the WDT STATUS register. This stops the clock to the WDT. You cannot disable the WDT unless you are in general-purpose timer mode or bus monitor mode.

9.0 SERIAL I/O UNIT

The Serial I/O unit (SIO) on the Intel386 EX embedded processor supports, much like the 80C186EB/EC, synchronous and asynchronous communications. Both processor families support independent baud-rate generator, programmable data frames, parity options, and break conditions for the transmitter and receivers, as well as support for receive and transmit interrupts. The Intel386 EX embedded processor also provides some enhanced features that include modem control support and diagnostics capabilities.

9.1 Asynchronous Serial I/O unit features and enhancements/ features

The Intel386 EX embedded processor asynchronous SIO unit supports two independent channels that are compatible with National Semiconductor's NSI16C450 and INS8250A. The asynchronous SIO units, support most of the asynchronous modes capabilities available on the 80C186EB/EC serial communication unit. This includes:

- Independent baud-rate generator,
- Clear to send feature for transmission.
- Break character transmission and detection.
- Parity, framing, and overrun errors
- Multiprocessing communication.
- Programmable data frames (start bit, 5 to 8 data characters, optional parity bit, 1 to 2 stop bits).
- Programmable parity (even, odd, forced, and no parity)
- Receive and transmit Interrupts.

The Intel386 EX embedded processor asynchronous SIO unit also supports some unique features that are not supported by the 80C186EB/EC. These features include modem control logic support, diagnostic mode capability, and enhanced receiver and transmitter interrupt support.

9.2 Asynchronous SIO Operation (SIO)

9.2.2 Baud-Rate Generator

The baud-rate generator on each asynchronous SIO channel can be clocked internally or externally, much like the 80C186EB/EC. For internal clocking, the serial clock (SERCLK = CLK2/4) is connected to the baud-rate generator input (BLKIN). For external clocking, the COMCLK is connected to the BLKIN input signal, The SIO configuration register (SIOCFG) must be configured to select either the internal or the external source. This corresponds to the BxCMP register on the 80C186EB/EC.

The baud-rate generator output is determined by BLKIN and a 16-bit divisor (8-bit on the 80C186EB/EC). Table 9-1 shows the baud-rate output frequencies.

9.2.3 Transmitter

The Intel386 EX embedded processor transmitter supports a programmable data frame that is similar to the one on the 80C186EB/EC (Table 9-2).

The Intel386 EX embedded processor transmitter supports the parity options available on the 80C186EB/EC including even, odd, or no parity. In addition, the Intel386 EX embedded processor transmitter can produce forced parity. Forced parity allows the SIO to be compatible with LAN protocol. The 80C186EB/EC break conditions are also supported on the Intel386 EX embedded processor transmitter.

The Intel386 EX embedded processor transmitter shifts the data to be transmitted out via the TXDn pin. The T X W and TXD1 pins are multiplexed with other functions. The pin configuration registers, PINCFG and P2CFG, must be configured properly to connect the TXDn signal to the package pin.

The transmitter also supports a transmitter empty (TE) and a transmit buffer empty (TBE) flags. This is a superset feature of the TXE bit feature available on the 80C186EB/EC.

Table 9-1. Baud-Rate Output Frequency

	Internal clock source	External clock Source
Intel386™ EX CPU	SERCLK, up to CLK2/4	COMCLK, up to 12.5 MHz
80C186EB/EC Baud-rate output freq.	CPU clock Intel386™ EX CPU. SERCLK/(16xdivisor) 80C186EB/EC, CPU/(8 × (divisor + 1))	BCLK, up to ½ CPU operating freq. Intel386™ EX CPU, BLKIN/(16 x divisor) 80C186EB/EC, BCLK/(8 x divisor)

Table 9-2. Transmitter Data Frame Programmable Elements

Prog. data frame	Start Bit	Data Char.	Parity Bit	Stop Bit
Intel386™ EX CPU	1	5 to 8	Optional	1 to 2
80C186EB/EC	1	7 to 9	Optional	1

Table 9-3. Receiver Data Frame Programmable Elements

Prog. data frame	Start Bit	Data Char.	Parity Bit	Stop Bit	Forced Parity
i386™ EX CPU	1	5 to 8	Optional	1 to 2	Yes
80C186EB/EC	1	7 to 9	Optional	1	No

9.2.4 Receiver

The Intel386 EX embedded processor receiver supports a programmable data frame that is similar to the one on the 80C186EB/EC (Table 9-3).

The Intel386 EX embedded processor receiver supports the parity options available'on the 80C186EB/EC including even, odd, or parity. In addition, it can produce forced parity. Forced parity allows the SIO to be compatible with LAN protocol.

The 80C186EB/EC break condition, parity errors, framing errors, and overrun errors are also supported on the Intel386 EX embedded processor receiver.

The Intel386 EX embedded processor receiver shifts the data in via the RXDn pin. The RXDO pin is multiplexed with another function. The pin configuration register, P2CFG, must be configured properly to connect RXDO signal to the package pin.

9.2.5 Modem Control

The Intel386 EX embedded processor supports modem control logic by providing the interfacing for four input signals (DSRn#, DCDn#, RIn#, and CTSn#) and two output signals (DTRn# and RTSn#) used for handshaking and status indication. This mode is not available on the 80C186 family.

9.2.6 Diagnostic Mode

The Intel386 EX embedded processor supports a diagnostic mode to aid in isolating faults in the communication link. This feature allows the Intel386 EX embedded processor to verify the internal transmit and receive paths of an SIOn channel. This feature is not available on the 80C186 family.

9.2.7 SIO Interrupt sources

The Intel386 EX embedded processor serial I/O unit (SIO) supports interrupts from four sources. The following table describes the sources and how they correspond to the 80C186EB/EC SCU interrupt sources (Table 9-4).

Table 9-4. SIO Interrupt Sources

Priority	Status Signal	Activated by	80C186EB/EC signal
1 (highest)	Receiver line status	Overrun, parity, or framing error, or break condition	Serial status register (SxSTS)
2	Receive buffer full	Receiver transferring data from its shift register to its buffer	RI bit in serial status register (SxSTS)
3	Xmit bufferempty	Transmitter transferring data from its transmit buffer to its transmit shift register	TI bit in serial status register (SxSTS)
4 (lowest)	Modem status	A change on any of the modem control input signals (CTS#, DCD#, DSR#, RI#) Not available.	N/A

10.0 SYNCHRONOUS SERIAL I/O UNIT

The Synchronous SIO unit (SSIO) on the Intel386 EX embedded processor is far more robust than the synchronous channel of the 80C186EB/EC (mode 0 synchronous mode). The SSIO supports 16-bit bi-directional serial communications, full duplex communications, as well as master and slave mode. The 80C186EB/EC is limited to 8-bit and half duplex communication and master mode only.

10.1 Synchronous SIO Operation (SSIO)

10.1.1 Baud-Rate Generator

In master mode, the baud-rate generator on the SSIO channel can be clocked internally from two different sources, PSCLK or SERCLK. The SIO configuration register (SIOCFG) must be configured to select either PSCLK or SERCLK to be connected to BLKIN of the baud-rate generator. On the 80C186EB/EC, the serial port can be clocked internally or externally and provides the synchronizing clock on its TXDn pin. The BxCMP register on the 80C186EB/EC must be configured to select internal or external clocking.

The baud-rate generator output on the Intel386 EX embedded processor is determined by BLKIN and a programmable baud-rate value (BV), which is the reload value for a 7-bit down counter. Table 10-1 shows the baud-rate output frequencies (master mode only) for the Intel386 EX embedded processor and the 80C186EB/EC.

10.1.2 Transmitter

The Synchronous SIOn on the Intel386 EX embedded processor supports much more functionality than the one available on the 80C186EC/B. For instance, the SSIO transmitter can operate in both master or slave modes, and hence supports full duplex communications. The 80C186EB/EC channels for synchronous communications operate in master mode only and can only support half duplex communications.

The SSIO shifts data out via its dedicated SSIOTX signal; whereas on the 80C186EB/EC, data is shifted in or out on the RXDn pin.

The transmitter supports a transmit holding buffer empty (THBE) flag and a transmit underflow error flag. When data is transferred from the buffer to the shift register, the THBE bit is set. This THBE bit feature is an improvement over the TXE bit available on the 80C186EB/EC. The TXE bit is set when both the holding buffer and the shift register are empty.

10.1.3 Receiver

The SSIO receiver can operate in both master or slave modes, therefore can support full duplex communications. The 80C186EB/EC channels for synchronous communications operate in master mode only and can only support half duplex communications.

The SSIO receiver shifts data in via its dedicated SSIORX signal; whereas on the 80C186EB/EC, data is shifted in or out on the RXDn pin.

The receiver supports a receive holding buffer full (RHBF) flag and a receive overflow error flag. When data is transferred from the shift register to buffer, the RHBF bit is set. This feature is not available on the 80C186EB/EC.

Table 10-1. Baud-Rate Output Frequencies

	Internal clock source	External clock Source
Intel386™ EX CPU	SERCLK, PSCLK	Not available
80C186EB/EC	CPU clock	BCLK, up to ½ CPU operating freq.
Baud-rate output freq.	Intel386 EX CPU, BCLKIN/(2BV + 2) 80C186EB/EC, (CPU/divisor) - 1	80C186EB/EC, BCLK/divisor

The programmable baud-rate value can be determined using the following equation:

$$BV = \left(\frac{BCLKIN}{2 \times BAUDRATE}\right) - 1$$

The divisor on the 80C186EB/EC is the baud-rate.

10.2 Programming the SIO

Five configuration registers, PI CFG, P2CFG, P3CFG, SIOCFG and PINCFG are provided in order to specify the connections for the SIO signals on the Intel386 EX embedded processor. These registers are not applicable to the SCU of the 80C186 family.

Table 10-2 lists the registers associated with SIO unit and the corresponding registers associated with the 80C186EB/EC.

Table 10-2. SIO Registers

Register	Function	80C186EB/EC register
PINCFG	connects TXD1, DTR1#, & RTSD1# to package pins	N/A
P1CFG	Connects RI0#, DSR0#, DTR0#, RTS0#, DCD0# to package pins	N/A
P2CFG	Connects CTS0#, TXD0, RXD0 to package pins.	N/A
P3CFG	Connects COMCLK to package pin	N/A
SIOCFG	Connects modem input signals internally or to package pins and connects either SERCLK or COMCLK to SIOn baud-rate generator.	N/A
DLLn	Stores the lower 8-bits of SIOn b-r generator divisor	Lower byte of BxCMP
DLHn	Stores the upper 8-bits of SIOn b-r generator divisor	Upper byte of BxCMP
TBRn	Holds the data byte for transmission	SxTBUF
RBRn	Holds the data byte received	SxRBUF
LCRn	Specifies the programmable data frame	Supports some bits of SxCON
LSRn	Contains transmitter empty, transmit buffer empty, receive buffer full, and receive error flags	Support SxSTS
IERn	Interrupt enable register	Support some bits of SxCON
IIRn	Indicates whether the modem status, transmit buffer empty, receive buffer full, or receive line status generated an interrupt request.	Support SxSTS
MCRn	Controls the interface with the modem or data set	N/A
MSRn	Provides current state of control lines for modem or data set	N/A
SCRn	8-bit read/write scratch pad register	N/A

11.0 INPUT/OUTPUT PORTS

Both the Intel386 EX embedded processor and the 80C186 family support up to three input/output ports. These ports can be configured as high-impedence inputs, open-drain outputs, or complementary outputs.

- Like the 80C186EC, the Intel386 EX embedded processor has three available 1/0 ports. The 80C186EB has only two available 1/0 ports.
- The Intel386 EX embedded processor has a maximum of 24 available I/O port pins. This is increased from the 22 I/O port pins available on the 80C186EC processor and the 16 I/O port pins available on the 80C186EB processor.
- The 1/0 port pins on the 80C186EB/EC processors and the Intel386 EX embedded processor processor are multiplexed with peripheral functions. The multiplexed functions on the Intel386 EX embedded processor are different from those on the 80C186EB/EC processors.
- The programming of the I/O port pins on the Intel386 EX processor is done in the same manner as on the 80C186EB/EC processors. Three registers are used to program the I/O port pin function: the Port Direction, Port Data Latch, and Port Pin State registers. The Port Control Register on the 80C186EB/EC processors configures the device pin for either an I/O port or a peripheral pin function. The Port Mode Configuration Register provides this functionality on the Intel386 EX processor.

11.1 Comparison of I/O Port Pins and Functionality

Table 11-1. I/O Port Pins and Functions

	Intel386 EX Processor	80C186EC	80C186EB
Port 1	8 pins configurable as: • high impedence input • open-drain output • complementary output	8 ouput-only pins	8 output-only pins
Port 2	8 pins configurable as: • high impedence input • open-drain output • complementary output	8 bidirectional port pins	• 1 bidirectional pin • 2 output-only pins • 3 input-only pins • 2 open-drain bidirectional pins (not multiplexed)
Port 3	8 pins configurable as: • high impedence input • open-drain output • complementary output	• 4 ouput-only pins • 2 open-drain bidirectional pins (not multiplexed)	Not available

11.2 I/O Port Pin Programming

The programming of the I/O pins on the Intel386 EX embedded processor is done in the same manner as on the 80C186 processors. The following registers are used, with a separate set of registers associated with each port.

- Port Control Register (80C186EB/EC)
  Port Mode Configuration Register (Intel386 EX embedded processor) — Controls whether the device pin is configured as an I/O port pin or as a peripheral pin.
- Port Direction Register — Sets the I/O port pin to function as either an input, a complementary ouput, or an open-drain output.
- Port Data Latch Register — For output pins, holds the value to be driven. For input pins or when not driving a zero on an open-drain output pin, places a high-impedence state on the I/O pin.
- Port Pin State Register — Allows the programmer to read the current pin state value.

Table 11-1 compares the I/O ports among the Intel386 EX, the 80C186EC and 80C186EB processors.

12.0 CHIP-SELECT UNIT

Both the 80C186 family and the Intel386 EX embedded processor's chip-select unit generate chip-selects for bus cycles initiated by the CPU, on-chip DMA controller, or on-chip refresh controller. The eight chip-selects' address blocks, wait state generation, and bus ready configurations are programmed independently of each other for maximum flexibility. With the Intel386 EX embedded processor's chip-select supporting the same features as the 80C186 family, a system designer will have no problem implementing chip-selects with the Intel386 EX embedded processor.

12.1 Intel386 EX Embedded Processor Chip-Select Unit Enhancements/ Features

The Intel386 EX embedded processor's chipselect unit supports the same features as the 80C186 family, but is more enhanced:

- eight independently programmable chip-selects
- chip-select disabling through software
- 2 byte *minimum I/O* address block resolution
- assertion (or deassertion) of the 8-bit bus control signal for 8- or 16-bit accesses
- access to multiple address blocks in a cycle

System Management Mode support

12.2 Chip-Select Configuration

Like the 80C186EB/EC microprocessor, the Intel386 EX embedded processor has an extremely programmable upper-memory chip-select and several independent, general-purpose chip-selects. Although the Intel386 EX embedded processor limits each block's starting address by an integer multiple of the block size, the chip-select unit has flexible address block rules.

Tables 12-1, 12-2, 12-3 and 12-4 list the available chip selects, address range, and selection scheme used by the different chip-select units.

Table 12-1. Upper Memory Chip Select

UCS #	Intel386 EX Embedded Processor	80C186/XL/EA	80C186EB/EC
On Reset	memoly-map enabled for 3FFFFFF–0000000H	memory-map enabled for OFFFF–OFFCOOH	memory-map enabled for OFFFF–OH
Memory-Mapped	2 KB block size 16 MB	1 KB block size 256 KB	1 KB block size 1 MB
	start addr = multiple of block size	start addr = multiple of block size end addr = OFFFFFH	start addr = multiple of 1 KB
I/O Mapped	2 bytes block size 64 KB	**N/A**	64 byte block size 64 KB
	start addr = multiple of block size	**N/A**	start addr = multiple of 64 bytes
Chip-Select Scheme	one chip-select mapped to one address block	one chip-select mapped to one address block	one chip-select mapped to one address block

Table 12-2. Lower Memory Chip Select

LCS#	Intel386™ EX Embedded Processor	80C186/XL/EA	80C186EB/EC
On Reset	N/A	disabled	disabled
Memory-Mapped	N/A	1 KB ≤ block size ≤ 256 KB	1 KB ≤ block size ≤ 1 MB
	N/A	start addr = 0H	start addr = multiple of 1 KB
I/O Mapped	N/A	N/A	64 byte ≤ block size ≤ 64 KB
	N/A	N/A	start addr = multiple of 64 byte
Chip-Select Scheme	N/A	one chip-select mapped to one address block	one chip-select mapped to one address block

Table 12-3. Mid-Range Memory Chip Selects

MCS3:0#	Intel386 EX Embedded Processor	80C186/XL/EA	80C186EB/EC
On Reset	N/A	disabled	N/A
Memory-Mapped	N/A	8 KB ≤ block size ≤ 512 KB	N/A
	N/A	start addr = multiple of block size	N/A
I/O Mapped	N/A	N/A	N/A
	N/A	N/A	N/A
Chip-Select Scheme	N/A	four chip-selects each mapped to one-fourth of a contiguous address block	N/A

Table 12-4. General-Purpose Chip Selects

General-Purpose	Intel386™ EX Embedded Processor	80C186/XL/EA	80C186EB/EC
On Reset	disabled	disabled	disabled
Memory-Mapped	2 KB ≤ block size ≤ 16 MB	block size ≤ 896 bytes	1 KB ≤ block size ≤ 1 MB
	start addr = multiple of block size	start addr = multiple of 1 KB	start addr = multiple of 1 KB
I/O Mapped	2 bytes ≤ block size ≤ 64 KB	block size = 896 bytes	64 byte ≤ block size ≤ 64 KB
	start addr = multiple of block size	start addr = multiple of 1 KB	start addr = multiple of 64 byte
Chip-Select Scheme	CS6:0#	PCS6:0#	GCS7:0#
	seven chip-selects each mapped to an independent address block(s)	seven chip-selects each mapped to one-seventh of a contiguous address block	eight chip-selects each mapped to an independent address block

12.3 Chip-Select Programming

Like the 80C186EB/EC microprocessors, the Intel386 EX embedded processor programs each chip-select independently of the others. The Intel386 EX embedded processor chip-selects can also be enabled and disabled like the 80C186EB/EC chip-selects.

Like the 80C186/XL/EA microprocessors, the Intel386 EX embedded processor programs the address blocks using a starting address and a block size. The channel address is similar to the 80C186/XL/EA microprocessor's starting address. The channel mask determines the address block size, but also allows each chip-select to access more than one address block per bus cycle.

Seven of the eight Intel386 EX embedded processor chip-selects are multiplexed with other signals. Table 12-5 shows the programmable features of the different chip-select units.

Table 12-5. Programmable Chip-Select Unit Features

	Intel386™ EX Embedded Processor	80C186/XL/EA	80C186EB/EC
Address Block	Channel Address & Mask	Start Addr & Block Size	Start & Stop Addr
Ignore Stop Address	N/A	N/A	
Chip-Select Enable		N/A	
Wait States	0 to 31	0 to 3	0 to 15
Bus Ready			
Bus Cycle Selector			
Bus Size	8-bit or 16-bit data bus	N/A	N/A
SMM mode		N/A	N/A
Pin Selector	CS6# or REFRESH# CS5# or DACKO# CS4:0# or P2.4:0	PCS6:5# or latched A2:A1 MCS3,1:0# or coprocessor pins	N/A

12.4 Chip-Select Activation

The Intel386 EX embedded processor chip-selects are activated in the same manner as the 80C186 family. The chip-selects become active when the CPU, the on-chip Refresh Control Unit, or the on-chip DMA Control Unit issues a memory read, a memory write, an instruction prefetch, or an I/O read or write within a programmed address block while the chip-select is enabled.

12.5 Address Block Overlapping

When one or more address blocks overlap, the 80C186EB/EC and Intel386 EX embedded processor must compromise between the overlapping chip-selects' wait state and bus ready configurations. If one or more of the overlapping chip-selects relies on the bus ready, the minimum number of configured wait states will be asserted. The chip-select unit will then continue to insert wait-states until bus ready is active. If none of the overlapping chip-selects rely on the bus ready, then the maximum number of configured wait states are asserted before the chip-select unit automatically ends the bus cycle.

For example, if one chip-select is configured for 3 wait states/no bus ready and overlaps with another chip select configured for 7 wait states/no bus ready, the chip-select unit will insert 7 wait states and automatically complete the bus cycle. If one or both of the chip-selects are configured for bus ready, then the chip-select unit will insert 3 wait states and continue to insert wait states until bus ready is asserted.

13.0 REFRESH CONTROL UNIT

The Refresh Control Unit (RCU) on the 80C186 processors and the Intel386 EX processor simplifies the interface between the processor and a dynamic random access memory (DRAM) device by providing a way to generate the periodic refresh requests and refresh addresses required by the DRAM device.

The RCU on the Intel386 EX processor supports all of the functionality of the RCU on the 80C186 processors. This includes:

- The refresh interval is programmable.
- The interval down-counter is loaded with the programmed refresh interval, and it is then decremented once every clock cycle. The down-counter times out when it reaches one, triggering a refresh request to be generated. It is then reloaded with the programmed refresh interval, and the process is repeated.
- A refresh request is generated when the interval down-counter times out. Refresh requests are sent to the Bus Interface Unit which performs a refresh bus cycle. The refresh bus cycles have a higher priority than all other CPU bus cycles. They look exactly like memory read bus cycles, except that both of the byte enable signals are driven high.
- The RCU generates the refresh addresses for the DRAM device. The refresh addresses on the Intel386 EX are fully compatible with those on the 80C186 processors, but also support larger-sized DRAM devices with up to 2^{13} rows of memory. The refresh addresses are split into three parts:
  - The upper bits are set by the programmer and represent the base address.
  - The lower bits, excluding bit 0, are generated by the RCU. These bits represent the address of the row to be refreshed.
  - Bit 0 is fixed at 1 to signal a refresh bus cycle.

13.1 Intel386 EX Embedded Processor RCU Enhancements

The Intel386 EX processor RCU provides some enhancements over the RCU of the 80C186 processors. These enhancements provide support for larger-sized DRAM devices and are summarized below.

- The refresh request interval is programmable with up to a 10-bit value.
- The variable pan of the refresh address is increased to 13 bits in order to support DRAM devices with up to 2^{13} rows of memory.

13.2 General RCU Operation

13.2.1 Refresh Request Generation

In both the 80C186 processors and the Intel386 EX embedded processor, the interval down-counter is loaded from the Refresh Clock Interval Register and is decremented once every clock cycle. A 9-bit down-counter is used on the 80C186 processors, while the Intel386 EX embedded processor uses a 10-bit down-counter to handle longer programmed refresh request intervals. Each of the processors generates a time-out signal when the down-counter reaches one, and this causes the RCU to initiate a refresh request. The down-counter is then reloaded, and the process is repeated. If a second refresh request is initiated while a refresh request is pending on any of the processors, a refresh request will be lost.

13.2.2 Refresh Bus Cycles

The refresh bus cycles of the 80C186 processors and Intel386 EX processor look exactly like read cycles, except both byte enable signals are driven high. This corresponds to BHE#/RFSH# and A0 held high on the 80C186 processors, and BHE# and BLE# held high on the Intel386 EX processor.

13.2.3 Ending the Refresh Process

Like the 80C186 processors, once enabled, the DRAM refresh process on the Intel386 EX processor continues indefinitely until either the RCU is reprogrammed, a reset occurs, or the processor enters powerdown mode.

13.3 Refresh Address Generation

Like the 80C186 processors, the Intel386 EX processor's refresh (Figure 13-1) address consists of a fixed component (base address) pointing to the location in memory where the DRAM device resides, a variable component (row address) which cycles through the rows of the DRAM device, and a fixed component.

Intel386 EX processor

25 ... 14	13 ... 1	0
base address	row address	1

80C186EB/EC

19 ... 13	12 ... 1	0
base address	row address	1

80C186XL/EA

19 ... 13	12	10 ... 9	1	0
base address	0	row address	1	

Figure 13-1. Refresh Addresses

13.4 Programming the Refresh Control Unit

The programming of the RCU on the Intel386 EX embedded processor is done in the same manner as on the 80C186 processors. Three control registers are used to program the RCU, while a fourth provides useful information to the programmer. Some of the reserved bits on the 80C186 processor's registers are utilized in the Intel386 EX processor's registers, since the refresh addresses are larger and require more bits to be programmed. The registers are described below:

- **Refresh Control Register** — Enables the RCU and holds the current value of the interval counter.
- **Refresh Base Address Register** — Sets the base address of the DRAM device, indicating where the device resides in memory.
- **Refresh Clock Interval Register** — Sets the desired clock count between refresh cycles.
- **Refresh Address Register** — Used to view the current row address bits. This is not supported on the 80C186XL/EA processors

14.0 Direct Memory Access Controller Unit

Like the 801C86 family's DMA channels, the Intel386 EX embedded processor's two DMA channels are independently programmable and will accept requests from the internal timer/counter unit, internal serial ports, external devices, and software. Each channel will support any combination of memory and I/O transfers with the capability of using the Intel386 EX embedded processor's chip-select unit for device selection. The channels can be configured for any combination of 8-bit and 16-bit transfers at various bus priority levels. With minor upgrades, the same 80C186 DMA channel configuration can be implemented with the Intel386 EX embedded processor's DMA controller.

14.1 Intel386 EX Embedded Processor DMA Controller Enhancements/ Features

The Intel386 EX embedded processor's DMA controller supports the same features as the 80C186 family, but is more enhanced:

- Higher Performance
- Lower DMA Latency
- DMA acknowledge and End-of-Process signals
- One cycle fly-by transfer option
- New transfer modes like DMA chaining and demand mode
- More flexible, independent channel configuration

14.2 DMA External Requests

While the 80C186 family requires a minimum of four cycles to initiate a DMA transfer after the request line is asserted, the Intel386 EX embedded processor improves on DMA latency by not requiring additional cycles for synchronizer resolution.

The Intel386 EX embedded processor provides a DMA acknowledge signal (DACKn#), decreasing the amount of external logic needed for DMA transfers. If 80C186 compatibility is necessary, the DACKn# signals can be masked or disabled through software.

14.3 DMA Transfer Cycles

The Intel386 EX embedded processor has a much higher performance DMA controller than the 80C186 family. The Intel386 EX embedded processor's DMA controller can perform a data transfer in one/two cycles while the 80C186 family requires eight/ten cycles. The Intel386 EX embedded processor's DMA controller has two transfer options, two-cycle and fly-by.

14.3.1 Two-Cycle Transfer Option

The two-cycle transfer option requires one clock per data read and one clock per data write. Data from the source device is written into a four-byte temporary buffer. When the buffer is full, the data is written to the destination device. BY using the temporary buffer, the Intel386 EX embedded processor's DMA channels can transfer any combination of 8-bit and 16-bit data. The two-cycle option can be used for any combination of memory and I/O transfers.

14.3.2 Fly-by Transfer Option

Using the fly-by transfer option, each data transfer requires only one clock. Fly-by transfers are limited to data transfers between an external device and memory.

The Intel386 EX embedded processor increases DMA performance by using identical cycles for source- and destination-synchronized transfers. When the 80C186 family inserts idle cycles at the end of every destination-synchronized transfer, the performance is degregated and the transfer can be suspended by a lower priority bus request.

14.4 DMA Transfer Termination

A Intel386 EX embedded processor's DMA transfers can be terminated by terminal count, disabling the channel in software, or assertion of the End-Of-Process (EOP#) signal.

14.4.1 Terminal Count

Like the 80C186 family, a Intel386 EX embedded processor DMA transfer can be terminated when the byte count register decrements to terminal count. The Intel386 EX embedded processor's byte count register and terminal count have been enhanced. Refer to the *Intel386 EX Embedded Microprocessor Hardware Reference* for programming details.

	Intel386 EX Embedded Processor		80C186 Family
	fly-by transfer	*two-cycle* transfer	fetch/deposit transfer
data read	½ cycle	1 cycle	4 cycles
data write	½ cycle	1 cycle	4/6 cycles

Software Termination

Like the 80C186 family, the Intel386 EX embedded processor's DMA transfer can be terminated through software. Termination is accomplished by setting the channel enable bit in the DMA command register.

14.4.2 End-of-Process

Unlike the 80C186 family, the Intel386 EX embedded processor's DMA controller provides the End-Of- Process (EOPX) I/O signal. An external source can terminate a DMA transfer by asserting the EOPX signal. Using the EOPX signal, an external device can transfer an unspecified number of bytes. The DMA controller will assert the EOPX signal on terminal count.

The Intel386 EX embedded processor's DMA controller includes many modes of operation not included on the 80C186 family. In some of the modes, the channel must be reprogrammed after every transfer completion or termination. While in other modes, the channel can reprogram itself and begin another transfer. Refer to the ***Intel386 EX Embedded Microprocessor Hardware Reference*** for more information on the Intel386 EX embedded processor transfer modes.

14.5 DMA Interrupt Requests

Like the 80C186 family, the Intel386 EX embedded processor DMA channels can request an interrupt on transfer termination. In addition to an interrupt request on terminal count, the Intel386 EX embedded processor's DMA channel can issue an interrupt request on transfer terminations caused by EOPX assertion.

Both Intel386 EX embedded processor DMA channels connect directly to an internal interrupt request line. Because both channels connect to the same interrupt request line, the DMA interrupt status register must be read to find out which channel caused the interrupt.

14.6 DMA Transfer Suspension

An Intel386 EX embedded processor DMA transfer can be suspended by assertion of the NMI, masking the DRQn signal in software, or deassertion of the DRQn signal. Whether the DRQn signal is masked by software or deasserted externally, the transfer is suspended until it is unmasked or reasserted.

14.7 Bus Control Arbitration

Like the 80C186 family, the Intel386 EX embedded processor's DMA controller provides the ability to program the DMA channel's bus priority. In addition, the priority of an external bus master can be programmed in relation to the DMA channel priorities.

Refresh requests always have the highest priority. The bus master, DMA channel 0, and DMA channel I are programmed in either rotating priority or by indicating the lowest priority request.

14.8 DMA Peripheral Request Configuration

Like the 80C186 family, the Intel386 EX embedded processor can accept DMA requests from the on-chip timer/counter unit, serial ports, or external devices. But, the Intel386 EX embedded processor offers more flexible configuration options with each channel configured independently of the other (Table 14-1).

Table 14-1. DMA Configuration Options

Channel 0	• Timer/Counter Unit Counter X1, or • Synchronous Serial Port #0's receiver, or • Synchronous Serial Port #1's transmitter, or • Asynchronous Serial Port's transmitter, or • an external source connected to DRQ0
Channel 1	• Timer/Counter Unit's Counter #2, or • Synchronous Serial Port #0's transmitter, or • Synchronous Serial Port #1's receiver, or • Asynchronous Serial Port's receiver, or • an external source connected to DRQ1

The Intel386 EX embedded processor's DMA controller can accept requests from more than one timer/counter and from different halves (transmit/receive) of any of the three serial ports. Unlike the 80186, one channel's configuration does not limit the other channel's configuration.

14.9 Additional Intel386 EX Embedded Processor DMA Features

Additional DMA features of the Intel386 EX embedded processor are:

- If more than two DMA channels are needed, an external DMA device can be cascaded into one of the Intel386 EX embedded processor's DMA channels.
- The DMA controller's features are a super-set of the 8237A, and can be configured to operate in 8237A-compatible mode.
- The DRQO, DRQ1, DACK0#, DACK1#, and EOPX signals are muliplexed with DCDI#, RXDI, CS5#, TXD1, and CTS1# signals, respectively. Because of the muliplexing, a few of the serial port features cannot be implemented if the DMA features are fully implemented.

15.0 Numerics Coprocessor

The Intel386 EX embedded processor provides an interface for the Intel387 SX numeric floating-point coprocessor. The hardware handshaking is supported via three processor signal pins: BUSY#, ERROR#, and PEREQ. The polarity of these signals are reversed when compared with the 80C186 family signals.

Both the Intel387 SX numeric floating-point coprocessor and the 80C187 conform to ANSI/IEEE Standard 754-1985. This means that the Intel387 SX will execute any code written for the 80C187 and vice versa.

The Intel386 EX embedded processor EX, unlike the 80C186 family, does not support a dedicated numerics chip select. However, this can be achieved without any external additional logic. Note that the Intel387 SX coprocessor interface addresses are beyond the 0H-OFFFFH range for programmed I/O. The math coprocessor is selected when the CPU issues one of the following I/O addresses, 8000F8H, 8000FCH, or 8000FEH. The Intel387 SX has two numeric processor select signals, NPS!# and NPS2. NPS1# should be tied directly to the M/IO# of the Intel386 EX embedded processor EX. This will insure that the Math Coprocessor is selceted only when the CPU performs I/O cycles. NPS2 should be connected directly to the A23 pin of the CPU, so that the math coprocessor is selected only when the CPU issues one of the I/O addresses reserved for the math coprocessor (8000F8H, 8000FCH, or 8000FEH).

To correctly map the Intel387 SX coprocessor registers to the appropriate I/O addresses, connect the CMDO and CMD1 lines to the A2 signal of the Intel386 EX embedded processor and to ground respectively.

16.0 SYSTEM MANAGEMENT MODE OVERVIEW (SMM)

The Intel386 EX embedded processor provides a mechanism for system management via a combination of hardware and CPU microcode enhancements. SMM was not implemeted on the 80C186 family, and as such, it will not be discussed in greater detail. For more information on SMM, please refer to the Intel386™ EX ***Embedded Processor Hardware Reference Manual,*** order number 272485.

Through the use of SMM, the system designer has a new method of adding software controlled features that operate transparently to the operating system and applications software. SMM is composed of a special purpose interrupt (SMI#) that serves as the hardware interface and a secure memory address space (SMRAM) that stores the processor status and special software routines. SMRAM is only available to the CPU during SMM mode and the software routines can be designed to control the power states of system components.

The SMI# input signal is used to invode SMM. It is similar to NMI where it is not maskable, is recognized on an instruction boundary, does not break LOCK'ed bus cycles, cannot interrupt currently executing SMM code, and will bring the processor out of idle or power-down mode.

Once SMM has been invoked, the CPU will respond by asserting a special SMM signal (SMIACT#). This signal is used by the system to enable the SMRAM space, where the processor will save its state. Once the CPU completes saving its state, it will be directed to an absolute address where it will begin executing the special software routines, including system power control.

The last instruction in any special software routine is the RSM instruction. This instruction will restore the processor state from the SMRAM space and return control of the system to the interrupted program.

17.0 JTAG TEST-LOGIC UNIT

The Intel386 EX embedded processor provides testability features compatible with the IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Sdt.1149.1). JTAG support was not implemeted on the 80C186 family, and as such, we will not discuss this subject in greater detail. For more information on JTAG, please refer to the *Intel386™* EX ***Embedded Processor Hardware Reference Manual,*** order number ***272485.***

The test logic unit on the *Intel386* EX Embedded processor allows for testing to insure that components function properly, that interconnections between various components are correct, and that various components interact correctly on the printed circuit board.

The boundary scan test logic consists of a boundary scan register and support logic that are accessed through a test access port (TAP). The TAP provides a simple serial interface that makes it possible to test all signal traces with only a few strobes.

The TAP can be controlled via a bus master, the bus master can be either automatic test equipment or a PLD that interfaces to the four-pin test bus.

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